CLAIMS

1. An integrated circuit assembly comprising:

a semiconductive substrate comprising a plurality of field effect transistors having electrically coupled sources and electrically coupled drains comprising regions of the substrate adjacent to a surface of the substrate, and wherein the electrically coupled sources and the electrically coupled drains are collectively configured to conduct power currents in excess of one Ampere; and

a package having a plurality of source contacts and a plurality of drain contacts configured to couple with the electrically coupled sources and the electrically coupled drains of the semiconductive substrate, and wherein the source contacts and the drain contacts are provided adjacent to the surface of the package.

2. The assembly of claim 1 wherein the semiconductive substrate further comprises a plurality of source contacts and a plurality of drain contacts coupled with respective ones of the sources and the drains of the field effect transistors, and wherein the source contacts and the drain contacts of the package are configured to couple with respective ones of the source contacts and the drain contracts of the power semiconductor switching device.

3. The assembly of claim 1 further comprising at least one metallization layer coupled with the substrate and configured to couple at least some of the sources in parallel and at least some of the drains in parallel.

4. The assembly of claim 3 wherein the semiconductive substrate further comprises a horizontal interconnect layer formed upon and coupled with the at least one metallization layer, and the horizontal interconnect layer defines a plurality of source contacts and a plurality of drain contacts configured to couple with respective ones of the source contacts and the drain contacts of the package.

5. The assembly of claim 1 wherein the package comprises at least one horizontal interconnect layer to provide the source contacts and the drain contacts.

6. The assembly of claim 1 wherein all electrical connections intermediate the sources and the drains of the substrate and the source contacts and the drain contacts of the package pass through the surface of the substrate.

7. The assembly of claim 1 wherein the package includes one terminal source contact and one terminal drain contact electrically coupled with respective ones of the source contacts and the drain contacts of the package and adapted to electrically couple with devices external of the semiconductor switching device.

8. The assembly of claim 7 wherein the package provides a plurality of electrical paths intermediate the one terminal source contact and the one terminal drain contact and respective ones of the source contacts and the drain contacts of the package, and the electrical paths individually have a resistance less than 1 milliOhm.

9. The assembly of claim 1 wherein the semiconductive substrate comprises a flip chip semiconductive die.

10. The assembly of claim 1 wherein the source contacts and the drain contacts of the power semiconductor device are arranged in alternating columns, and wherein the package comprises a vertical laminate package comprising a plurality of conductive layers corresponding to respective ones of the columns.

11. The assembly of claim 1 wherein the package comprises at least one horizontal interconnect layer.

12. The assembly of claim 11 wherein the at least one horizontal interconnect layer is spaced from the power semiconductor device; and further comprising a plurality of electrical interconnects intermediate the horizontal interconnect layer and the source contacts and the drain contacts of the power semiconductor device.

13. The assembly of claim 1 wherein the number of source contacts of the power semiconductor device is less than the number of sources and the number of drain contacts of the power semiconductor device is less than the number of drains.

14. The assembly of claim 1 wherein the semiconductive substrate comprises a monolithic substrate including the field effect transistors and auxiliary circuitry.

15. The assembly of claim 1 wherein the semiconductive substrate comprises a monolithic substrate including the field effect transistors and auxiliary circuitry coupled with the plurality of field effect transistors.

16. The assembly of claim 1 wherein the field effect transistors comprise MOSFET devices.

17. An integrated circuit assembly comprising:

a power semiconductor switching device comprising:

a semiconductive substrate having a surface; and

a power transistor formed using the substrate and having a plurality of source contacts and drain contacts adjacent to the surface and configured to conduct power currents; and

a package having a plurality of source contacts and a plurality of drain contacts corresponding to and electrically coupled with respective ones of the source contacts and the drain contacts of the power semiconductor device.

18. The assembly of claim 17 wherein the power transistor comprises a plurality of planar field effect transistors.

19. The assembly of claim 17 wherein the power transistor comprises a plurality of planar field effect transistors coupled in parallel.

20. The assembly of claim 17 further comprising at least one metallization layer coupled with the substrate and configured to couple at least some of the source contacts in parallel and at least some of the drain contacts in parallel.

21. The assembly of claim 20 further comprising a horizontal interconnect layer formed upon and coupled with the at least one metallization layer, and the horizontal interconnect layer defines the source contacts and the drain contacts of the power transistor.

22. The assembly of claim 17 wherein the package comprises at least one horizontal interconnect layer to provide the source contacts and the drain contacts of the package.

23. The assembly of claim 17 wherein all electrical connections intermediate the source contacts and the drain contacts of the substrate and the source contacts and the drain contacts of the package pass through the surface of the substrate.

24. The assembly of claim 17 wherein the power transistor is configured to conduct power currents in excess of one Ampere.

25. The assembly of claim 17 wherein the package includes one terminal source contact and one terminal drain contact electrically coupled with respective ones of the source contacts and the drain contacts of the package and adapted to electrically couple with devices external of the semiconductor switching device.

26. The assembly of claim 25 wherein the package provides a plurality of electrical paths intermediate the one terminal source contact and the one terminal drain contact and respective ones of the source contacts and the drain contacts of the package, and the electrical paths individually have a resistance less than 1 milliOhm.

27. The assembly of claim 17 wherein the semiconductive substrate comprises a flip chip semiconductive die.

28. The assembly of claim 17 wherein the source contacts and the drain contacts of the power semiconductor device are arranged in alternating columns, and wherein the package comprises a vertical laminate package comprising a plurality of conductive layers corresponding to respective ones of the columns.

29. The assembly of claim 17 wherein the package comprises at least one horizontal interconnect layer.

30. The assembly of claim 29 wherein the at least one horizontal interconnect layer is spaced from the power semiconductor device; and further comprising a plurality of electrical interconnects intermediate the horizontal interconnect layer and the source contacts and the drain contacts of the power semiconductor device.

31. The assembly of claim 17 wherein the number of source contacts of the power semiconductor device is less than the number of sources and the number of drain contacts of the power semiconductor device is less than the number of drains.

32. The assembly of claim 17 wherein the semiconductive substrate comprises a monolithic substrate including the field effect transistors and auxiliary circuitry.

33. The assembly of claim 17 wherein the semiconductive substrate comprises a monolithic substrate including the field effect transistors and auxiliary circuitry coupled with the plurality of field effect transistors.

34. The assembly of claim 17 wherein the power transistor comprises a plurality of MOSFET devices.

35. A power semiconductor switching device packaging method comprising:

providing a semiconductive substrate having a surface;

forming a power transistor having plurality of source contacts and a plurality of drain contacts using the semiconductive substrate and adjacent to the surface;

providing a package having a plurality of source contacts and a plurality of drain contacts corresponding to the source contacts and drain contacts of the power transistor; and

coupling the source contacts and the drain contacts of the power transistor with the source contacts and the drain contacts of the package.

36. The method of claim 35 wherein the forming the power transistor comprises forming a plurality of planar field effect transistors.

37. The method of claim 35 wherein the forming the power transistor comprises forming a plurality of planar field effect transistors coupled in parallel.

38. The method of claim 35 further comprising forming at least one metallization layer to couple at least some of the source contacts of the power transistor in parallel and to couple at least some of the drain contacts of the power transistor in parallel.

39. The method of claim 38 wherein the at least one metallization layer forms the source contacts and the drain contacts of the power transistor.

40. The method of claim 38 further comprising forming a horizontal interconnect layer upon the at least one metallization layer to form the source contacts and the drain contacts of the power transistor.

41. The method of claim 35 wherein the providing the package comprises providing at least one horizontal interconnect layer providing the source contacts and the drain contacts of the package.

42. The method of claim 35 wherein the coupling comprises coupling the source contacts and the drain contacts of the power transistor with the source contacts and the drain contacts of the package to pass all electrical signals communicated intermediate the power transistor and the package through the surface of the semiconductive substrate.

43. The method of claim 35 wherein the forming comprises forming the power transistor to conduct power currents in excess of one Ampere.

44. The method of claim 35 wherein the providing the package comprises providing the package having a single source terminal contact and a single drain terminal contact.

45. The method of claim 35 wherein the providing the semiconductive substrate comprises providing a semiconductive die having a flip chip configuration.

46. The method of claim 35 wherein the forming the power transistor comprises forming the power transistor having the source contacts and the drain contacts arranged in alternating columns.

47. The method of claim 46 wherein the providing the package comprises providing the package having the source contacts and the drain contacts arranged in a plurality of conductive layers corresponding to the columns.

48. The method of claim 35 wherein the providing the package comprises providing the package having at least one horizontal layer coupled with the source contacts and the drain contacts of the package.

49. The method of claim 35 wherein the providing the semiconductive substrate comprises providing a monolithic semiconductive substrate, and further comprising forming auxiliary circuitry using the monolithic semiconductive substrate.

50. The method of claim 35 wherein the providing the semiconductive substrate comprises providing a monolithic semiconductive substrate, and further comprising forming auxiliary circuitry coupled with the power transistor.

51. The method of claim 35 wherein the forming comprises forming the power transistor to comprise a plurality of MOSFET devices.

52. A power semiconductor switching device packaging method comprising:

providing a semiconductive substrate comprising a plurality of planar field effect transistors coupled in parallel and collectively configured to conduct currents in excess of one Ampere;

providing a package having a plurality of source contacts and a plurality of drain contacts; and

coupling the source contacts and the drain contacts with the planar field effect transistors.

53. The method of claim 52 wherein the providing the semiconductive substrate comprises providing the semiconductive substrate comprising the planar field effect transistors having a plurality of source contacts and a plurality of drain contacts configured to couple with respective ones of the source contacts and the drain contacts of the package.

54. The method of claim 52 further comprising forming at least one metallization layer upon the surface of the semiconductive substrate to couple at least some of the planar field effect transistors in parallel.

55. The method of claim 54 wherein the forming comprises forming the at least one metallization layer to define a plurality of source contacts and a plurality of drain contacts configured to couple with respective ones of the source contacts and the drain contacts of the package.

56. The method of claim 54 further comprising forming at least one horizontal interconnect layer upon the at least one metallization layer to form a plurality of source contacts and a plurality of drain contacts to couple with respective ones of the source contacts and the drain contacts of the package.

57. The method of claim 52 wherein the providing the package comprises providing the package including at least one horizontal interconnect layer configured to provide the source contacts and the drain contacts.

58. The method of claim 52 wherein the providing the package comprises providing the package having a single source terminal contact and a single drain terminal contact.

59. The method of claim 52 wherein the coupling comprises coupling the source contacts and the drain contacts of the package with the field effect transistors to pass all electrical signals communicated intermediate the field effect transistors and the package through a surface of the semiconductive substrate.

60. The method of claim 52 wherein the providing the semiconductive substrate comprises providing a semiconductive die having a flip chip configuration.

61. The method of claim 52 wherein the providing the semiconductive substrate comprises providing the semiconductive substrate having a plurality of source contacts and a plurality of drain contacts arranged in alternating columns.

62. The method of claim 61 wherein the providing the package comprises providing the package having the source contacts and the drain contacts arranged in a plurality of conductive layers corresponding to the columns.

63. The method of claim 52 wherein the providing the package comprises providing the package having at least one horizontal layer coupled with the source contacts and the drain contacts of the package.

64. The method of claim 52 wherein the providing the semiconductive substrate comprises providing a monolithic semiconductive substrate having auxiliary circuitry.

65. The method of claim 52 wherein the providing the semiconductive substrate comprises providing a monolithic semiconductive substrate having auxiliary circuitry coupled with the field effect transistors.

66. The method of claim 52 wherein the providing the semiconductive substrate comprises providing the semiconductive substrate comprising the planar field effect transistors implemented as MOSFET devices.

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